A Physically Based Analytic Model of FET Class-E Power Amplifiers—Designing for Maximum PAE

David K. Choi, *Student Member, IEEE*, and Stephen I. Long, *Senior Member, IEEE*

Abstract— In this paper, we present a new Class-E power-amplifier model. Through a physically based analysis, our novel approach yields closed-form expressions for input, output, and dc power. These expressions yield the important figures-of-merit [gain, drain efficiency, and power-added efficiency (PAE)]. Using standard device parameters, design optimization for maximum PAE follows directly from the analysis and applies to both integrated and discrete transistor implementations. For integrated designs, the optimal FET aspect ratio can be determined, given the design variables of the Class-E output network (output power, frequency, supply voltage, and loaded-Q of the output resonator). In a discrete transistor application, the Class-E network can be optimized for one of the design variables. The detrimental effects of the device parasitics on the amplifier's performance at UHF and microwave frequencies are accounted for in the model and explained in this paper. We verified the validity of the model by comparing our computed values against those from simulations using an optimized 0.5-μm CMOS level-3 SPICE model.

Index Terms— CMOSFET power amplifiers, FET amplifiers, microwave power FET amplifiers, MOSFET power amplifiers, switching amplifier, UHF power amplifiers.

I. INTRODUCTION

THE recent proliferation of the wireless (cellular) communication industry has rekindled interest in the Class-E tuned power amplifier for high-efficiency transmitter applications. Most of the recent work focuses on practical design issues, but for the most part, neglects theoretical analyses that could explain some of the difficulties encountered at high frequencies.

The lack of new theoretical treatments may be attributable in part to the fact that the switched-mode operation of the Class-E amplifier does not lend itself easily to conventional circuit analysis techniques. Additionally, there exists an extensive collection of theoretical work by Sokal and Sokal [1], Raab and Sokal [2], Kazimierczuk [3], [4], Kazimierczuk and Puczko [5], and Raab [6].

The single-transistor Class-E amplifier topology, shown in Fig. 1, consists of an FET, RF choke, and output network comprised of a shunt capacitor and a series *RLC* circuit that appears inductive at the driving frequency. Thorough derivations and explanations of the Class-E operation condition (nonsimultaneous high drain current and voltage) exist in the literature [1]–[6]. Waveforms for the drain current and voltage and their associated mathematical expressions are shown in
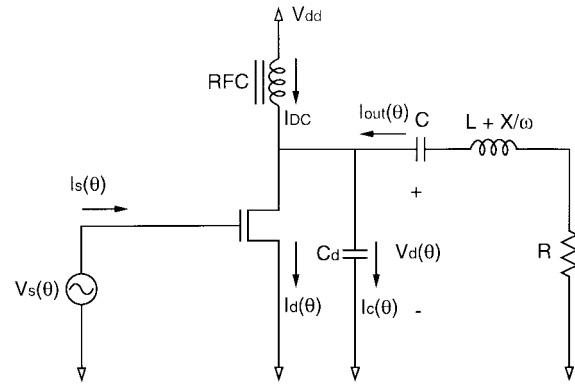
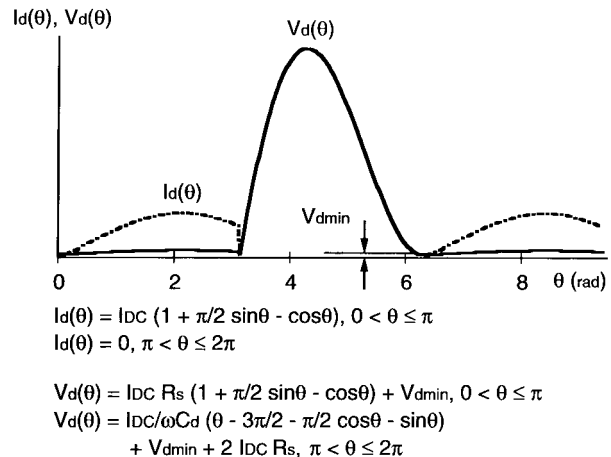Fig. 1. Single-ended FET Class-E resonant tuned power amplifier.

$$I_d(\theta) = I_{DC}(1 + \pi/2 \sin\theta - \cos\theta),\ 0 < \theta \leq \pi$$
$$I_d(\theta) = 0,\ \pi < \theta \leq 2\pi$$

$$V_d(\theta) = I_{DC} R_s (1 + \pi/2 \sin\theta - \cos\theta) + V_{d\min},\ 0 < \theta \leq \pi$$
$$V_d(\theta) = I_{DC}/\omega C_d (\theta - 3\pi/2 - \pi/2 \cos\theta - \sin\theta)$$
$$+ V_{d\min} + 2 I_{DC} R_s,\ \pi < \theta \leq 2\pi$$

Fig. 2. Class-E drain current and voltage waveforms and equations (V_d and I_d are the duals of those from [3], $V_{d\min}$ and $I_d(\theta)R_s$ are new in this analysis).

Fig. 2 [3]. In Fig. 2, we added additional terms to account for the voltage drop across the source resistance and for the finite drain voltage during conduction ($V_{d\min}$). The values of the output network elements for Class-E operation are given in Table I [1].

A priori designability (i.e., the Class-E amplifier can be designed without knowledge of the transistor's characteristics) was shown to be valid at low frequencies (3.9 MHz) [1], but it is not generally realizable. At high frequencies, the device parasitics and resultant degradation in transconductance severely impact the circuit's performance. Consequently, the ideal switch model of the transistor (which is the foundation of the *a priori* approach) needs to be reevaluated.

In order to develop an accurate high-frequency model, our approach takes into account the device parasitics and

TABLE I
CLASS-E DESIGN EQUATIONS [1]
Class E Output Network Design Equations

P_{out}	Design output power	$\dfrac{\pi^2+4}{8} I_{DC}^2 R$
R	Load resistance	$\dfrac{8V_{dd}^2}{P_{out}(\pi^2+4)}$
X/ω	Excess inductance	$\dfrac{\pi V_{dd}^2(\pi^2-4)}{2\omega P_{out}(\pi^2+4)}$
L	Resonator inductor	$\dfrac{8Q_L V_{dd}^2}{\omega P_{out}(\pi^2+4)}$
C	Resonator capacitance	$\dfrac{P_{out}(\pi^2+4)}{8\omega V_{dd}^2 Q_L}$
C_d	Shunt capacitance	$\dfrac{P_{out}}{\pi\omega V_{dd}^2}$

the finite transconductance of the transistor. In addition, our model overcomes the ambiguity in analyzing the switched-mode operation of the active device in the Class-E amplifier. We make the analysis of the physical operation of the device tractable by applying separate models for the on and off states of the transistor. In the computations, we use device parameters from the level-3 SPICE model (see the Appendix) and measured values for the parasitic resistances that were not included in the SPICE model.[1]

Despite the large body of existing works (to the best knowledge of the authors), no one has considered the effect of the parasitic elements present on the input side of the Class-E amplifier until now. Furthermore, we propose a new explanation for the effect of the series source resistance.

In what follows, we will demonstrate that *a priori* design of MOSFET Class-E amplifiers does not apply at cellular band frequencies (900 MHz). It will become apparent that the nonideal characteristics of the active device play a substantial role in the performance of the amplifier. Therefore, we will examine how the parasitics and marginal high-frequency transconductance of n-channel MOSFET's affect gain and drain efficiency.

We will show that simultaneous high gain and drain efficiency are difficult to achieve using this device technology at these frequencies. Consequently, power-added efficiency (PAE), rather than drain efficiency, will be used as the appropriate figure-of-merit. We will also present a method for determining the optimal FET aspect ratio that yields maximum PAE given a Class-E output network designed for a particular set of design parameters. Using essentially the same approach, we will also show that given a particular aspect ratio (the case of a discrete FET), it is possible to find the optimal output power at which to design the Class-E network.

II. A New Class-E Amplifier Model

The ideal switch model becomes inadequate to describe the performance of the Class-E amplifier as the operating

[1] The MOSIS Service, "MOSIS parametric test results," Run N8AK, Vendor: HP, Feature size: 0.5 μ\m, File: N8AK. [Online]. Available HTTP: http://www.mosis.org/html/hp-amos14tb-prm.html

frequency increases. First, it neglects the input power required to drive the active device. Therefore, in general, the ideal switch model cannot be used to estimate gain. Additionally, it fails to model the transistor's finite transconductance. This omission leads to inaccurate drain efficiency estimates at high frequencies.

The ideal switch model is based on the premise that the active device has zero resistance while conducting current. The characteristic high transconductance and low-source terminal resistance of a wide channel device allow for low drain voltage during conduction. The *a priori* approach, therefore, suggests that it is always best to use an FET with an extremely high aspect ratio.

However, as the driving frequency increases, a large FET will require considerable drive power to charge and discharge its substantial input capacitance. Even at high frequencies, a Class-E amplifier using a large device may yield high drain efficiency. The problem is that this amplifier will most likely have low gain.

On the other hand, using a significantly smaller device to drive the same Class-E output network will require less input power and, therefore, may have higher gain. However, its lower transconductance, higher source terminal resistance, and resultant higher drain voltage during conduction will lower its drain efficiency.

Clearly there is a tradeoff between high gain and high drain efficiency. In our analysis, we examine how the transistor's parasitics and limited transconductance affect gain and drain efficiency. By formulating expressions for input, output, and dc power, we construct a coherent model that allows optimization for maximum PAE.

The following analysis is restricted to FET's. A detailed analysis for bipolar transistor Class-E amplifiers is the topic of a future paper. In this analysis, we assume that the parasitic capacitances are proportional to channel width and that the resistive parasitics scale inversely with the width dimension. We assume that the length of each gate finger is fixed and that the FET is laid out in an interdigitated structure. Our other assumptions include: ideal load transformation (to meet the Class-E design value, see Table I), 50% duty-cycle, loaded-Q of five, ideal reactive elements, and only linear capacitors.

A. Input Power

The input power derived here is the input power delivered to the input circuit. The source is represented in Figs. 1 and 3(a)–(c) by the ideal voltage source V_s.

Fig. 3(a) shows the equivalent circuit of the FET Class-E amplifier with the relevant parasitics. Instead of an ideal switch, our model employs a finite transconductance element for the active device. In order to simplify the analysis, the source terminal resistance is bypassed for the gate-to-source and drain-to-source capacitances. The comparisons of the relevant computations (input power, output power, PAE, etc.) show that connecting these capacitances directly to ground does not significantly impact the accuracy of our model.

The source terminal resistance (R_s) consists of interconnect resistances (ohmic contact resistance, bond wires, and leads).
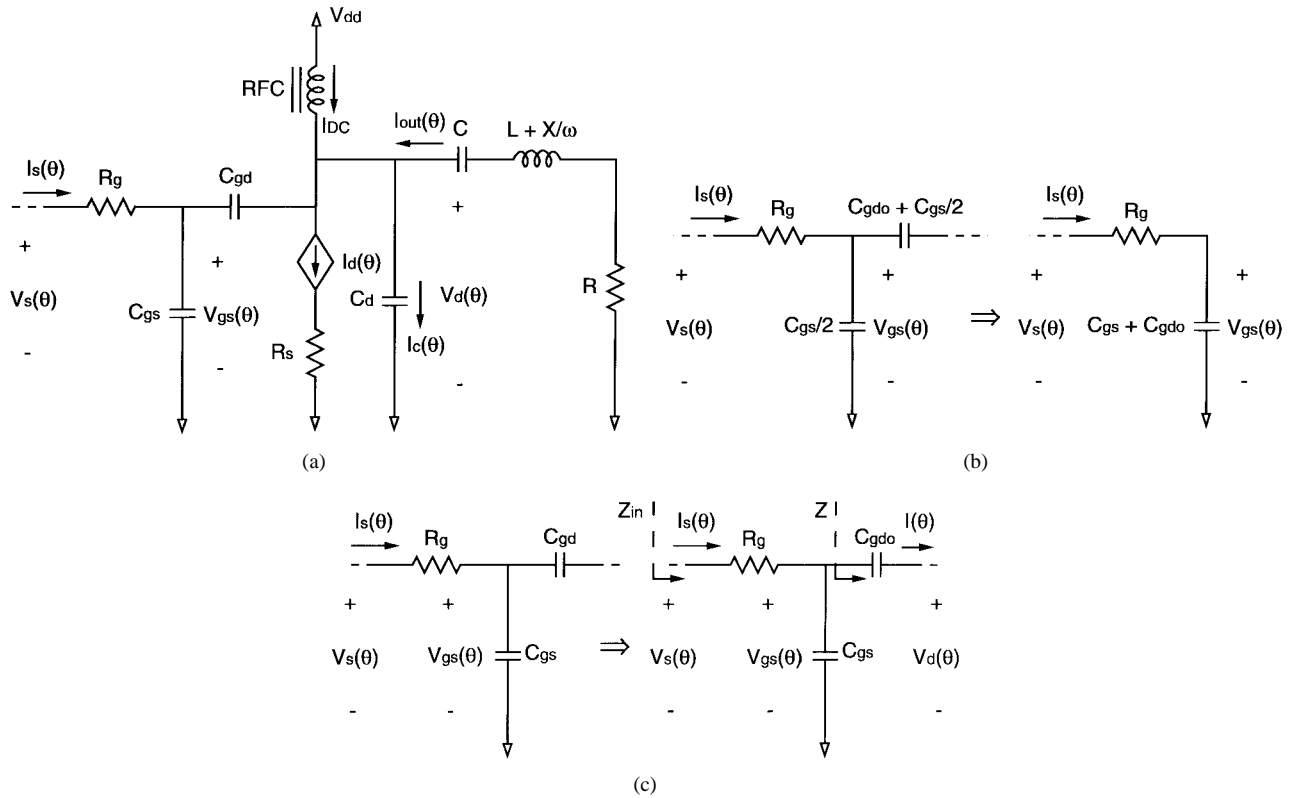
Fig. 3.   (a) Complete equivalent FET Class-E amplifier circuit. (b) Equivalent input circuit for positive half of input cycle (R_s neglected). (c) Equivalent input circuit for negative half of input cycle (R_s neglected).

The series gate resistance (R_g) has the same constituents as the source resistance, but also includes the poly-silicon sheet resistance.

The value of the gate-to-drain bridging capacitance (C_{gd}) depends on the FET's mode of operation. When the FET is cut off, C_{gd} consists of only the overlap capacitance (C_{gdo}). When the conductive channel is enhanced between the source and drain, C_{gd} consists of C_{gdo} plus half of C_{gs}.

In order to give a 50% duty-cycle, the device is dc biased at its threshold voltage. Thus, during the positive-going half of the sinusoidal input ($0<\theta \leq \pi$), the FET is active, and during the negative half ($\pi<\theta \leq 2\pi$), it is cut off. We perform the input power calculation in separate parts to model the switched-mode operation of the device. Each part of the analysis uses a different equivalent circuit representing either the active or cutoff state of the FET.

1) Positive Half of the Input Cycle ($0<\theta \leq \pi$)*:* For simplicity, we assume that the drain voltage is constant during the positive half of the cycle. This allows us to add C_{gd} and C_{gs} in parallel. The input circuit then simplifies to a series connection of a resistor and capacitor [see Fig. 3(b)]. The power drawn during this interval is as follows:

$$P_{\mathrm{in1}} = \frac{1}{4}\mathrm{Re}\left[V_s I_s^*\right] = \frac{V_s^2}{4}\frac{R_g\left[\omega(C_{\mathrm{gs}} + C_{\mathrm{gdo}})\right]^2}{1 + \left[\omega R_g(C_{\mathrm{gs}} + C_{\mathrm{gdo}})\right]^2}. \quad (1)$$

2) Negative Half of the Input Cycle ($\pi<\theta \leq 2\pi$)*:* The gate-to-drain bridging capacitance makes this calculation more complicated. While the FET is cut off, no current flows

through the device. The current flowing in the shunt capacitor (C_d) generates a voltage pulse on the drain (Fig. 2). We approximate the drain voltage with a sinusoidal pulse of amplitude equal to that of the actual pulse. Thus, the impedance looking into the bridging capacitor [see Fig. 3(c)] is given as

$$Z = \frac{V_{\mathrm{gs}}}{I} = \frac{V_{\mathrm{gs}}}{j\omega C_{\mathrm{gdo}}(V_{\mathrm{gs}} + V_{d\max})}. \quad (2)$$

The maximum drain voltage ($V_{d\max}$) can be computed from the voltage equation given in Fig. 2 as follows:

$$V_{d\max} = 1.13\frac{I_{\mathrm{DC}}}{\omega C_d} + V_{d\min} + 2I_{\mathrm{DC}}R_s. \quad (3)$$

The gate-to-source voltage is written as

$$V_{\mathrm{gs}} = \frac{V_s}{1 + \dfrac{R_g}{Z} + j\omega R_g C_{\mathrm{gs}}}. \quad (4)$$

Substitution of (2) into (4) yields an expression for V_{gs} in terms of V_s and the other quantities. The current (I_s) flowing into the circuit is simply the difference between V_s and V_{gs} divided by R_g [see Fig. 3(c)]. The power drawn during the negative half-cycle can then be expressed as

$$P_{\mathrm{in2}} = \frac{V_s}{4}\frac{\omega^2 R_g(C_{\mathrm{gs}} + C_{\mathrm{gdo}})}{1 + \left[\omega R_g(C_{\mathrm{gs}} + C_{\mathrm{gdo}})\right]^2}$$
$$\times \left[V_s(C_{\mathrm{gs}} + C_{\mathrm{gdo}}) + V_{d\max}C_{\mathrm{gdo}}\right]. \quad (5)$$

Spice Parameters and Sheet Resistance

K'	Intrinsic transconductance	$2.00 \times 10^{-4}\,(A/V^2)$
μ	Bulk mobility	$546\,(cm^2/Vs)$
C_{GDO}	Gate to drain overlap cap.	$3.05 \times 10^{-10}\,(F/m)$
ρ_{gate}	Poly-silicon sheet resistance	$1.9\,(\Omega/square)$
r_m	Metal resistance	$0.07\,(\Omega/square)$
r_c	Metal-Poly contact resistance	$1.8\,(\Omega/gate\ finger)$

Fig. 4. Input power (900 MHz, 1 W) versus number of gate fingers.

Finally, the total power delivered by the source is the sum of (1) and (5) as follows:

$$P_{\text{in}} = \frac{V_s}{4} \frac{\omega^2 R_g (C_{\text{gs}} + C_{\text{gdo}})}{1 + \left[\omega R_g (C_{\text{gs}} + C_{\text{gdo}})\right]^2} \times \left[2V_s(C_{\text{gs}} + C_{\text{gdo}}) + V_{d\max} C_{\text{gdo}}\right]. \quad (6)$$

Since we assume that the FET has an interdigitated structure, it is more natural to express the resistance and capacitances in (6) as functions of the number of gate fingers n. We define the width and length of a single finger as W and L, respectively. By doing this, the gate capacitances will be directly proportional to the number of fingers. The gate resistance will be inversely proportional to n, except for the fixed packaging and interconnect resistance r_m. These expressions are given as follows:

$$R_g = r_m + \frac{1}{n}\left(\frac{\rho_{\text{gate}} W}{3L} + r_c\right) = r_m + \frac{r_g}{n}$$
$$C_{\text{gs}} = n\frac{K'WL}{\mu} = nc_{\text{gs}}$$
$$C_{\text{gdo}} = nC_{GDO}W = nc_{\text{gdo}}. \quad (7)$$

In (7), $K'(A/V^2)$ and μ (cm²/V/s) are the SPICE model parameters for intrinsic transconductance and bulk carrier mobility, respectively. C_{GDO} is the SPICE parameter for the gate-to-drain capacitance per unit gatewidth. The poly-silicon sheet resistance is denoted by ρ_{gate} (Ω/square), and r_c (Ω/finger) is the metal-to-poly contact resistance. The factor of 1/3 for the gate resistance provides an equivalent lumped resistance for the distributed RC network [7]. The values of the parameters above were taken from the optimized level-3 SPICE model, and the measured values of ρ_{gate}, r_c, and r_m are from MOSIS (Table II).

Now we can re-express the input power in terms of n as follows:

$$P_{\text{in}} = \frac{\omega^2 V_s}{4} \frac{n(nr_m + r_g)(c_{\text{gs}} + c_{\text{gdo}})}{1 + \omega^2(n^2 r_m^2 + 2nr_m r_g + r_g^2)(c_{\text{gs}} + c_{\text{gdo}})^2} \times \left[2V_s(c_{\text{gs}} + c_{\text{gdo}}) + V_{d\max} c_{\text{gdo}}\right]. \quad (8)$$

In general, the fixed resistance is much smaller than the other components of the gate resistance. By neglecting r_m, the input
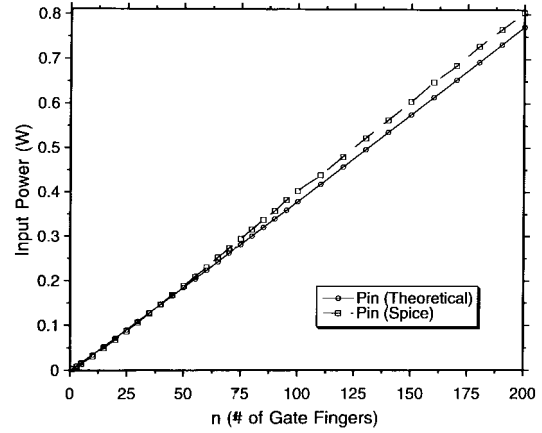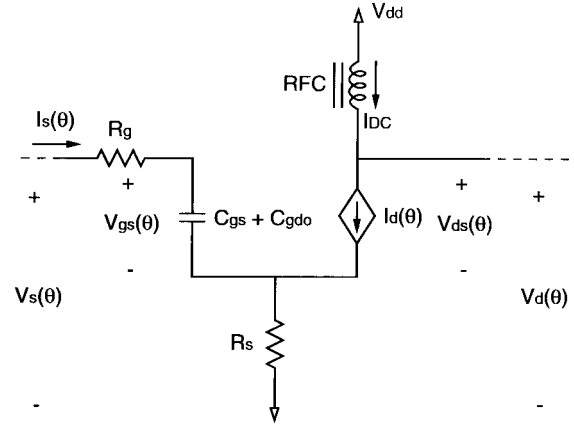

Fig. 5. Equivalent FET circuit including R_s.

power can be simplified to a linear function of n as follows:

$$P_{\text{in}} = \frac{n\omega^2 V_s}{4} \frac{r_g(c_{\text{gs}} + c_{\text{gdo}})}{1 + \left[\omega r_g(c_{\text{gs}} + c\text{gdo})\right]^2} \times \left[2V_s(c_{\text{gs}} + c_{\text{gdo}}) + V_{d\max} c_{\text{gdo}}\right]. \quad (9)$$

The plots of the simulated and modeled results [from (6)] for input power as a function of the number of fingers are indeed quite linear (Fig. 4). Both here and in what follows, the length and width of each finger will be assumed to be 0.5 and 125 μm, respectively.

B. DC Current in Terms of R_S—The Effect of R_S

In our analysis, we model the transistor as a voltage-controlled current source, where the controlling voltages are the gate-to-source and the drain-to-source voltages. This model allows us to compute the dc current drawn by the circuit as well as the finite drain-to-source voltage during conduction ($V_{d\min}$).

Since the drain of the FET is connected to the dc supply by an RF choke, the average drain voltage must equal the supply voltage. Integration of the drain voltage [here, the $I_d(\theta)R_s$ drop must be included (see Fig. 5)] over one cycle, and some algebraic manipulation yields the following expression for
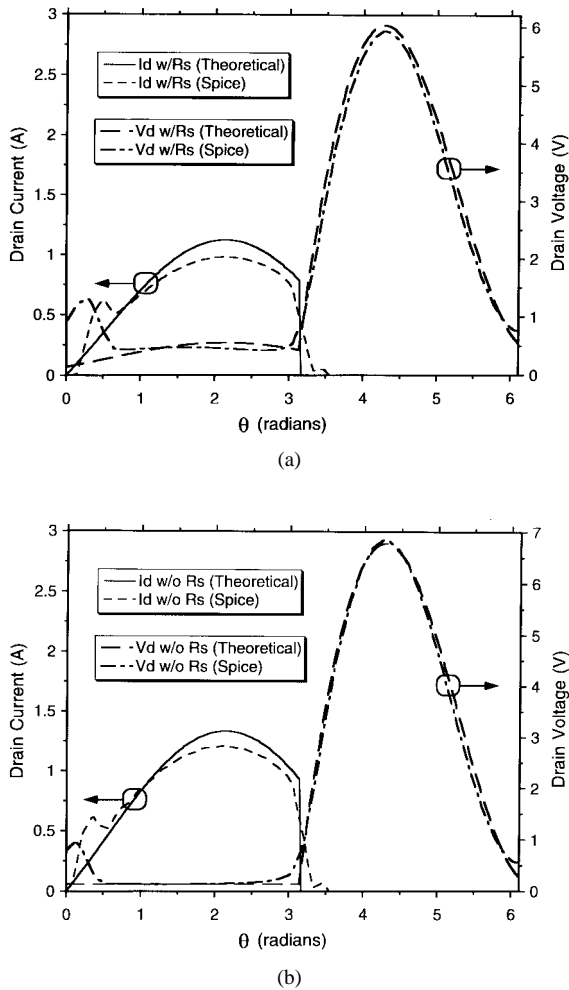
(a)

(b)

Fig. 6.　(a) Drain current and voltage waveforms with R_s. (b) Drain current and voltage waveforms without R_s.

I_{DC}:

$$\left\langle V_d(\theta) \right\rangle = \frac{1}{2\pi} \left[\int_0^\pi \left(V_{d\min} + I_d(\theta) R_s \right) d\theta \right.$$
$$\left. + \int_\pi^{2\pi} \left(V_d(\theta) + V_{d\min} + I_d(\pi) R_s \right) d\theta \right]$$
$$= V_{dd}$$
$$\Rightarrow \; I_{\mathrm{DC}} = \frac{\pi\omega C_d (V_{dd} - V_{d\min})}{1 + 2\pi\omega R_s C_d}. \qquad (10)$$

This expression shows how the dc current is affected by the source resistance. The plots of the drain current and voltage in Fig. 6(a) and (b) illustrate that the *source resistance is not simply a dissipative element*, as assumed earlier in the literature [2], [8]. Instead, it also has the effect of limiting the dc current drawn from the supply.

1) Computing $V_{d\min}$: The minimum drain voltage ($V_{d\min}$) remains as an unknown in (10). It can be computed by solving the FET drain current equation for $V_{d\min}$. We defined $V_{d\min}$ as the drain-to-source voltage during conduction; hence,

$$V_{\mathrm{ds}}(\pi) = V_{d\min}. \qquad (11)$$

Assuming that the FET remains in the triode region ($V_{\mathrm{ds}} \leq V_{\mathrm{gs}} - V_t$), the familiar FET current equation relates the drain current to V_{gs} and V_{ds} as follows:

$$I_d(\pi) = \frac{K'W}{2L} \left[2V_{\mathrm{gs}}(\pi) V_{\mathrm{ds}}(\pi) - V_{\mathrm{ds}}(\pi)^2 \right] = 2I_{\mathrm{DC}}. \qquad (12)$$

The amplitude and phase of the gate-to-source voltage relative to the input voltage (V_s) can be computed from the equivalent circuit shown in Fig. 5

$$|V_{\mathrm{gs}}'| = \frac{|V_s|}{\sqrt{1 + \left[\omega(R_g + R_s)(C_{\mathrm{gs}} + C_{\mathrm{gd}}) \right]^2}},$$

$$\angle V_{\mathrm{gs}}' = \chi = \arctan\left[-\omega(R_g + R_s)(C_{\mathrm{gs}} + C_{\mathrm{gd}}) \right] \qquad (13)$$

$$V_{\mathrm{gs}}(\theta) = |V_{\mathrm{gs}}'| \sin(\theta + \chi) - I_d(\theta) R_s. \qquad (14)$$

Initially, the voltage drop across R_s due to $I_d(\theta)$ is neglected in the derivation of (13), but is later accounted for in (14). After substituting (10), (11), and (14) in (12) and collecting terms, the solution for $V_{d\min}$ is just that of a quadratic as follows:

$$V_{d\min} = -\frac{b + \sqrt{b^2 - 4ac}}{2a}$$
$$a = 1 - 2\pi\omega R_s C_d$$
$$b = 2\left[2\pi\omega R_s C_d \left[V_{dd} - V_{\mathrm{gs}}(\pi) \right] \right.$$
$$\left. - 2\pi\omega C_d \frac{L}{K'W} - V_{\mathrm{gs}}(\pi) \right]$$
$$c = 4\pi\omega C_d \frac{L}{K'W} V_{dd}. \qquad (15)$$

2) DC Power: The dc power is simply the product of (10) with the supply voltage

$$P_{\mathrm{DC}} = I_{\mathrm{DC}} V_{dd} = \frac{\pi\omega C_d (V_{dd} - V_{d\min})}{1 + 2\pi\omega R_s C_d} V_{dd}. \qquad (16)$$

The plot of (16) in Fig. 7(a) shows how the dc power varies with n.

C. Output Power

In order to compute the power delivered to the load, we first calculate the output current. The current flowing in the output resonator shown in Fig. 1 is the sum of the FET and shunt capacitor currents minus the dc current. Since we are primarily interested in the fundamental component of the output current, Fourier analysis will produce the desired coefficients.

The output current must be computed in separate parts as well. Again, we will analyze the two regimes corresponding to the active and cutoff modes of the FET.

1) Output Current ($0 < \theta \leq \pi$): During this interval, the device current is described by the equation given in Fig. 2. The current flowing in the shunt drain capacitor is proportional to the derivative of the drain voltage (Fig. 2)

$$I_c(\theta) = \omega C_d \frac{dV_d(\theta)}{d\theta} = \omega C_d I_{\mathrm{DC}} R_s \left(\frac{\pi}{2} \cos\theta + \sin\theta \right). \qquad (17)$$
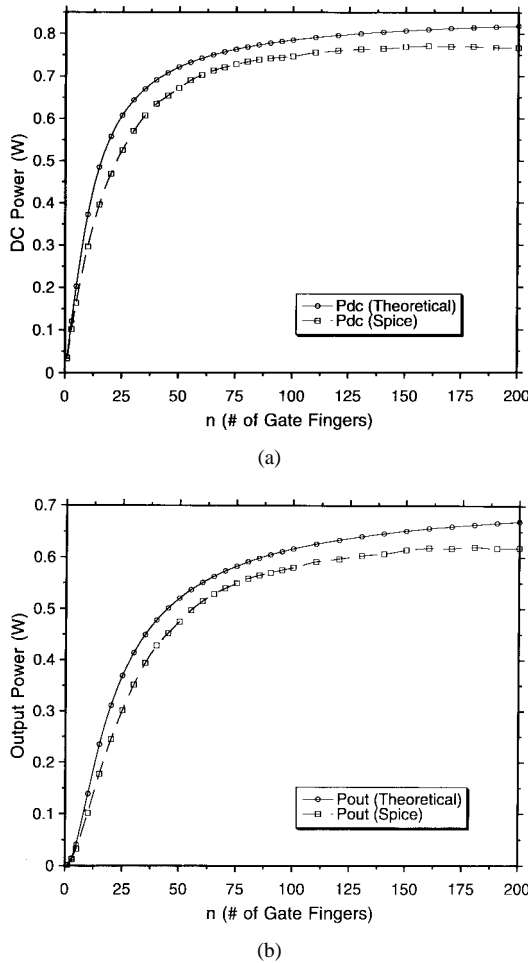
Fig. 7. (a) DC power (900 MHz, 1 W) versus number of gate fingers. (b) Output power (900 MHz, 1 W) versus number of gate fingers.

Using (17), the output current during the first half-cycle becomes

$$
\begin{aligned}
I_{\text{out}}(\theta) &= I_d(\theta) + I_c(\theta) - I_{\text{DC}} \\
&= I_{\text{DC}} \left[\left(\frac{\pi}{2} + \omega R_s C_d \right) \sin\theta + \left(\frac{\pi \omega R_s C_d}{2} - 1 \right) \cos\theta \right].
\end{aligned}
$$

$$(18)$$

2) Output Current $(\pi < \theta \le 2\pi)$: While the FET is cut off $(\pi < \theta \le 2\pi)$, the device current is zero and, once again, the shunt capacitor current is equal to the derivative of the voltage across the shunt capacitor

$$
I_c(\theta) = I_{\text{DC}} \left(1 + \frac{\pi}{2} \sin\theta - \cos\theta \right), \qquad \pi < \theta \le 2\pi. \quad (19)
$$

Here, the output current is

$$
\begin{aligned}
I_{\text{out}}(\theta) &= I_c(\theta) - I_{\text{DC}} \\
&= I_{\text{DC}} \left(\frac{\pi}{2} \sin\theta - \cos\theta \right), \qquad \pi < \theta \le 2\pi. \quad (20)
\end{aligned}
$$

3) Fourier Analysis: The $I_d(\theta) R_s$ voltage drop during the conduction interval introduces a quadrature component to the sinusoidal output current. Therefore, the cosine term should be included in the analysis although its contribution to the output power may be relatively small.

A phase shift (ϕ) between the switching cycle and the output current arises from derivation of the drain current [6]. This phase must be included in the analysis since it arises from the derivation of Class-E equations [1].

The sine and cosine of this phase angle are the useful quantities in the derivation of the output power expression

$$
\sin\varphi = -\frac{2}{\pi^2 + 4} \qquad \cos\varphi = \frac{\pi}{\pi^2 + 4}. \quad (21)
$$

Using (18), (20), and (21), we can compute the Fourier integrals.

$$
\textit{Cosine Term:} \quad a_1 = \frac{1}{\pi} \int_0^{2\pi} I_{\text{out}}(\theta) \cos(\theta + \varphi) \, d\theta \quad (22)
$$

$$
\Rightarrow a_1 = \frac{I_{\text{DC}} \omega R_s C_d}{4} \sqrt{\pi^2 + 4}. \quad (23)
$$

The sine term is calculated in an analogous fashion.

$$
\textit{Sine Term:} \quad b_1 = \frac{1}{\pi} \int_0^{2\pi} I_{\text{out}}(\theta) \sin(\theta + \varphi) \, d\theta \quad (24)
$$

$$
\Rightarrow b_1 = \frac{I_{\text{DC}} \sqrt{\pi^2 + 4}}{2}. \quad (25)
$$

With these coefficients, the output current at the fundamental is

$$
I_{\text{out}}(\theta)|_{\text{fundamental}} = a_1 \cos(\theta + \varphi) + b_1 \sin(\theta + \varphi). \quad (26)
$$

Finally, the output power becomes

$$
P_{\text{out}} = \frac{1}{2} |I_o(\theta)|^2 R = \frac{\pi^2 + 4}{8} I_{\text{DC}}^2 R \left[1 + \left(\frac{\omega R_s C_d}{2} \right)^2 \right]. \quad (27)
$$

If the source resistance is neglected, the output power reverts back to the form originally derived in [1] (Table I). The plot of the output power versus the number of gate fingers in Fig. 7(b) shows that, beyond a certain limit, there is little advantage in using larger devices. In fact, since the input power increases almost linearly with the number of gate fingers, using an excessively large FET will adversely affect gain. It is also interesting to note that the inclusion of (10) in (27) eliminates the need for a separate calculation of the power dissipated in R_s. This reduction in output power is automatically taken into account in (27).

III. DESIGN OPTIMIZATION

Now that the power relationships have been derived, we are prepared to compute gain, drain efficiency, and PAE. As we proceed with the derivations, we will show that an FET that produces high gain may suffer from low drain efficiency and vice versa. Consequently, our methodology entails finding the best compromise between gain and drain efficiency, i.e., we optimize the design for maximum PAE.
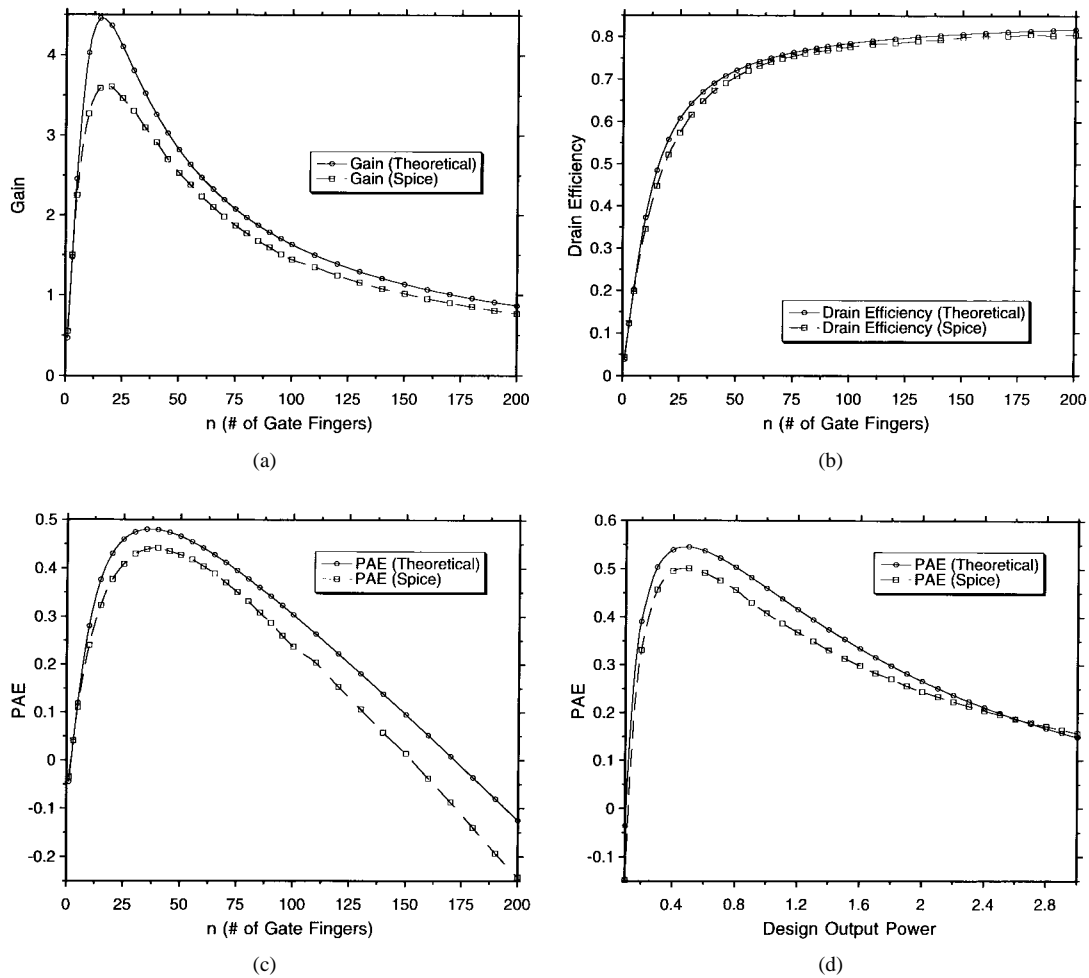
Fig. 8. (a) Gain (900 MHz, 1 W) versus number of gate fingers. (b) Drain efficiency (900 MHz, 1 W) versus number of gate fingers. (c) PAE (900 MHz, 1 W) versus number of gate fingers. (d) PAE (900 MHz) versus designed output power: 25 gate fingers ($W/L = 125$ μm/0.5 μm).

A. Gain

To be precise, we are referring to operating power gain since the input power is derived in (6) and the output power in (27) is the power delivered to the load. The operating power gain is, therefore, the ratio of (27) and (6), shown in (28), at the bottom of the page. As would be expected from the plots of input and output power, the plot of gain versus number of MOSFET gate fingers exhibits a definite peak [see Fig. 8(a)].

B. Efficiency

Even for devices with sufficient transconductance, the harmonic distortion, output network losses, and source terminal resistance of the FET prevent the drain efficiency from reaching 100%. Nevertheless, attaining reasonably high drain efficiency ($\geq 70\%$) is not very difficult. It is the difficulty

in achieving high gain that is problematic. Therefore, we emphasize the importance of achieving high PAE rather than high drain efficiency.

1) Drain Efficiency: Like output power, drain efficiency increases rapidly with the number of gate fingers, and then levels off [see Fig. 8(b)]. This should not be surprising since, qualitatively, we would expect that the larger the device is, the more closely it approximates an ideal switch. Quantitatively, the drain efficiency is the ratio of the output power to dc power as follows:

$$\text{Efficiency} = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{I_{\text{DC}}R(\pi^2+4)\left[1+\left(\dfrac{\omega R_s C_d}{2}\right)^2\right]}{8V_{dd}}. \tag{29}$$

$$\text{Gain} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_{\text{DC}}^2 R(\pi^2+4)\left[1+\left(\dfrac{\omega R_s C_d}{2}\right)^2\right]\left(1+[\omega R_g(C_{\text{gs}}+C_{\text{gdo}})]^2\right)}{2V_s\omega^2 R_g(C_{\text{gs}}+C_{\text{gdo}})\left[2V_s(C_{\text{gs}}+C_{\text{gdo}})+V_{d\max}C_{\text{gdo}}\right]} \tag{28}$$

$$\begin{aligned}
\text{PAE} &= \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \\
&= \text{Efficiency} - \frac{P_{\text{in}}}{P_{\text{DC}}} \\
&= \frac{I_{\text{DC}} R (\pi^2 + 4)\left[1 + \left(\frac{\omega R_s C_d}{2}\right)^2\right]}{8 V_{dd}} - \frac{V_s \omega^2 R_g (C_{\text{gs}} + C_{\text{gdo}})\left[2 V_s (C_{\text{gs}} + C_{\text{gdo}}) + V_{d\max} C_{\text{gdo}}\right]}{4 I_{\text{DC}} V_{dd}\left(1 + \left[\omega R_g (C_{\text{gs}} + C_{\text{gdo}})\right]^2\right)}
\end{aligned} \qquad (30)$$

2) PAE: Finally, we compute the PAE using its standard definition, shown in (30), at the top of the page. A comparison [see Fig. 8(a)–(c)] shows that the value of n that will produce maximum PAE lies between the relatively low value for the peak gain and the high value of n where the drain efficiency approaches its limit.

Fig. 8(d) illustrates how (30) can be applied to a device with a fixed number of fingers (the case of a discrete FET). Here, the output power parameter from the Class-E equations (Table I) is the independent variable.

IV. PRACTICAL DESIGN CONSIDERATIONS

It has been suggested previously that the transistor's parasitic drain-to-source capacitance can be absorbed in the shunt capacitor of the output network [1]. MOSFET devices typically have large gate-to-drain parasitic capacitances as well. The additional contribution to the drain-to-source capacitance made by the gate-to-drain component should be reflected in C_d.

$$\begin{aligned}
C_d' &= C_d - C_{\text{ds}} - C_{\text{gd}} \\
&= \frac{P_{\text{out}}}{\pi \omega V_{dd}^2} - C_{\text{ds}} - C_{\text{gdo}}.
\end{aligned} \qquad (31)$$

In (31), the shared capacitance $(C_{\text{gs}}/2)$ does not appear as part of C_{gd} since the drain capacitor plays a role in the operation of the Class-E circuit primarily while the device is off.

V. CONCLUSION

Our analysis uses the original design equations for the Class-E output network as a starting point. Our first departure from the *a priori* approach was to model the effects of the input parasitics. This led the way to the formulation of an expression for the input power. We next applied a finite-transconductance model instead of the ideal switch. By using the FET current equation, we established a mathematical relationship between the device terminal voltages and drain current. This was a crucial step in our approach since it provided a way of computing I_{DC}, which strongly affects the output power. Ultimately, we derived an expression for PAE which, in this case, serves as an indicator of how well the active device and Class-E network are suited for one another.

In essence, our design approach is an extension of the *a priori* method. However, our technique insures an optimal design by analyzing how the realistic behavior of the device affects the overall performance of the amplifier.

APPENDIX

The optimized level-3 SPICE model parameters for the 0.5-μm CMOS devices are as follows.

.param v_{to}	0.6566;
.param u_o	546.2182;
.param θ	0.2684;
.param η	$3.000e - 03$;
.param ld	$4.700e - 08$;
.param δ	0.6900;
.param n_{fs}	$5.900e + 11$;
.param tox	$9.600e - 09$;
.param c_{gdo}	$3.052e - 10$;
.param c_{gbo}	$4.024e - 10$;
γ	0.5976;
$v_{\max}$	$2.000e + 05$;
κ	$2.898e - 02$;
r_{sh}	35.0011;
kp	$2.000e - 04$;
xj	$2.000e - 07$;
ϕ	0.7000;
n_{sub}	$1.392e + 17$;
c_{gso}	$3.052e - 10$;
cj	$5.620e - 04$.

REFERENCES

[1] N. O. Sokal and A. D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168–176, June 1975.

[2] F. H. Raab and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 912–914, Dec. 1978.

[3] M. Kazimierczuk, "Class E tuned power amplifier with shunt inductor," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 2–7, Feb. 1981.

[4] ——, "Effects of the collector current fall time on the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 181–193, Apr. 1983.

[5] M. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switching duty cycle," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 149–159, Feb. 1987.

[6] F. H. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, pp. 725–735, Dec. 1977.

[7] P. H. Ladbrooke, *MMIC Design: GaAs FET's and HEMT's.* Norwood, MA: Artech House, 1989.

[8] C. Li and Y. Yam, "Analysis and design of the class E amplifier with non-zero ON resistance," *Microwave Opt. Technol. Lett.*, vol. 7, pp. 337–341, May 1994.

David K. Choi (S'98) received the B.A. degree in physics from the University of California at Berkeley, in 1993, and the M.S. degree in electrical engineering from California State University, Fullerton, in 1996, and is currently working toward the Ph.D. degree at the University of California at Santa Barbara

While with the Western Digital Corporation and Adaptec Corporation, he participated in digital cell characterization. Since joining the Department of Electrical and Computer Engineering, University of California at Santa Barbara, his work has centered around high-efficiency power amplifiers for wireless communications.

Stephen I. Long (S'68–M'73–SM'80) received the B.S. degree in engineering physics from the University of California at Berkeley, in 1967, and the M.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1969 and 1974, respectively.

From 1974 to 1977, he was a Senior Engineer and Manager of Semiconductor Engineering at Varian Associates, Palo Alto, CA. From 1978 to 1981, he was a Member of Technical Staff at Rockwell International Science Center, Thousand Oaks, CA. In 1981, he joined the Electrical and Computer Engineering Department, University of California at Santa Barbara, where he is currently a Professor. In 1988, he was a Research Visitor at GEC Hirst Research Centre, U.K. In 1994, he was a Fulbright Research Visitor at the Signal Processing Laboratory, Tampere University of Technology, Finland, and a Visiting Professor at the Electromagnetics Institute, Technical University of Denmark. His research interests include the design of low-power high-speed digital and analog circuits, integrated circuit (IC) interconnections, high-performance devices and fabrication technologies, and microwave analog IC's for personal communications.

Dr. Long received the 1978 IEEE Microwave Applications Award for development of InP millimeter-wave devices.