Finite DC Feed Inductor in Class E Power Amplifiers—A Simplified Approach

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Abstract— **This report describes a method for using a finite DC feed inductor in place of an (infinite inductance) RF choke. In addition to providing the DC feed connection, the finite feed inductor can be used to perform two other functions needed in the Class E power amplifier topology, namely, transformation of the 50Ω load and reactive tuning. Since no assumptions are made about the shunt output capacitor, this result is independent of the capacitor's voltage dependence. The analysis results in simple, elegant, and easy to use design equations that, in the limit where the feed inductor approaches infinity, reverts to the case with the RF choke. The concept was demonstrated using a silicon LDMOS FET operating at $200MHz$.**

I. Introduction

USING a finite DC feed inductor instead of an RF choke has the advantages of smaller size, lower loss, and greater ease in realizability. The value of using a finite DC feed inductor in Class E power amplifiers has apparently been recognized by many authors, as evidenced by the large number of reports on this subject.

Zulinski made the first significant attempt to study this topic by applying Laplace transform techniques to solve the integro-differential equation used to describe the system [1]. In subsequent publications Zulinski examined the effect of finite feed inductance and arbitrary loaded-Q of the output network [2], as well as the effect of the finite feed inductor in the series-capacitor rendition of the Class E topology [3]. Avratoglou et al. also studied the finite feed inductor in the series-capacitor Class E topology [4] and analyzed the effect of a finite feed inductor in the shunt-capacitor Class E with arbitrary loaded-Q and finite ON resistance [5]. However, Zulinski and Avratoglou's analyses are based on Laplace transforms which tend to be complicated because of the large number of coefficients that must be computed.

In [6] Li and Yam went a step further by imposing an explicit resonant condition between the feed inductor and the shunt output capacitor. However, their final solution relies on numerical solution which also lacks the intuition that is helpful in initial design.

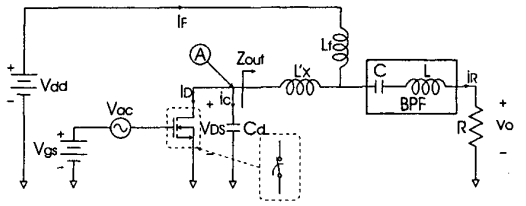

Fig. 1. Class E Power Amplifier with Finite DC Feed Inductor

The first well-defined, analytic solution for the finite feed inductor Class E amplifier was reported by Iwadare et al. [7]. Their approach is similar to that used by Li and Yam [6], but theirs results in analytic solutions because of the even harmonic resonant condition they imposed, i.e.,

$$\omega^2 L_f C_d = 2n, \tag{1}$$

where, $n = 1, 2, 3, \ldots$. The resulting analytic design equations are concise and intuitive. Furthermore, when $n = 1$, their approach results in a "critical frequency" for Class E operation [8], i.e., the frequency where the required output capacitance is made up entirely of the transistor's parasitic capacitance, four times greater than when an RF choke is used.

Unfortunately, the optimal load resistance using Iwadare's approach is over an order of magnitude smaller than with an RF choke [7]. Small values of load resistance (on the order of a few ohms) are difficult to realize accurately and are detrimental to efficiency as the parasitic resistances in the circuit approach a significant fraction (≈10 percent) of the total load resistance. So, while Iwadare's even harmonic approach is elegant and offers significant frequency extension, there is a penalty associated with the reduced load resistance. Finally, like the other approaches [1]–[6], the even harmonic technique is only applicable when the shunt output capacitor is linear.

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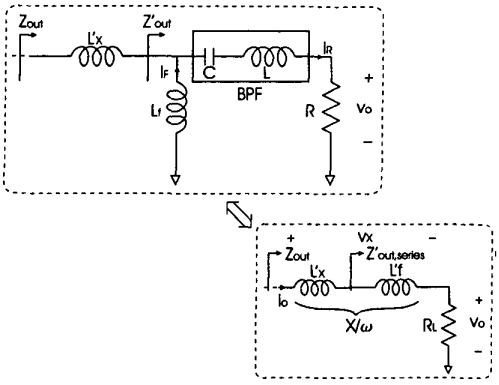

Fig. 2. AC Equivalent of Finite Feed Inductor Output Circuit

II. A Simplified Approach

Analytic design equations for the finite DC feed inductor can be found without resorting to Laplace transforms [1]–[5], numerical analysis [6], or even, to solving a second-order differential equation [7]. This analysis is simply based on the assumption that the series-LC output resonator has a Q_L high enough to allow only a sinusoidal current, $i_R(\theta)$ (see fig. 1).

A. Analysis

The feed inductor, L_f, carries *both* AC and DC currents but, as will be shown below, leaves the operation of the Class E circuit fundamentally unchanged. The AC component of $I_F(\theta)$ can be found from fig. 2, which shows that the AC voltage across L_f equals the AC voltage across the LC resonator and R_L. Under the high Q_L assumption,

$$i_R(\theta) = i_R \sin(\theta + \psi), \tag{2}$$

and therefore,

$$v_o(\theta) = i_R R \sin(\theta + \psi). \tag{3}$$

The total current flowing through L_f can be defined as

$$I_F(\theta) = I_{dc} + i_f(\theta), \tag{4}$$

where,

$$i_f(\theta) = -\frac{i_R R}{\omega L_f} \cos(\theta + \psi). \tag{5}$$

Now, referring back to fig. 1, summing the currents at node "A" results in

$$I_F(\theta) - i_R(\theta) = I_D(\theta) + i_C(\theta), \tag{6}$$

where the left side can be rewritten as

$$\begin{aligned} I_F(\theta) - i_R(\theta) &= I_{dc} - i_R\left[\sin(\theta)\left(\cos(\psi) - \frac{\sin(\psi)}{Q_f}\right)\right. \\ &\quad \left. + \cos(\theta)\left(\sin(\psi) + \frac{\cos(\psi)}{Q_f}\right)\right] \end{aligned} \tag{7}$$

where[1],

$$Q_f \equiv \frac{\omega L_f}{R}. \tag{8}$$

Equation (7) can be rewritten as

$$\begin{aligned} I_F(\theta) - i_R(\theta) &= I_{dc} - i_o \sin(\theta + \phi) \\ &= I_D(\theta) + i_C(\theta), \end{aligned} \tag{9}$$

which is the form obtained for the RF choke implementation, where

$$i_o \sin(\phi) = i_R\left(\sin(\psi) + \frac{\cos(\psi)}{Q_f}\right) \tag{10}$$

and

$$i_o \cos(\phi) = i_R\left(\cos(\psi) - \frac{\sin(\psi)}{Q_f}\right). \tag{11}$$

Therefore the design equations derived for the case of an RF choke are equally applicable here.

B. Class E Design Equations

Detailed derivations of the design equations[2] for $\langle C_{eff}\rangle$, R_L, and X are beyond the scope of this work, but they can be found in [9] and [10]. The design equations are simply given here, where y and σ are defined as: half of the *non*-conduction interval,

$$y \equiv \pi[1 - (duty - cycle)], \tag{12}$$

and the voltage slope at the onset of conduction, subject to the constraint[3],

$$\sigma \equiv \left.\frac{dV_{DS}(\theta)}{d\theta}\right|_{\theta_{on}} < -\alpha(y)\frac{I_{dc}}{\omega C_{jo}}, \tag{13}$$

respectively [9],[10].

$$\begin{aligned} \langle C_{eff}\rangle &\equiv \frac{\langle Q_{capacitor}(\theta)\rangle}{\langle V_{DS}(\theta)\rangle} \\ &= \frac{I_{dc}}{\pi\omega V_{dd}}\alpha(y)\left[\alpha(y) + \frac{\omega C_{jo}\sigma}{I_{dc}}\right] \end{aligned} \tag{14}$$

[1]Please note that Q_f should not be confused with $Q_L = \frac{\omega L}{R_L}$.
[2]Nonlinear capacitors can be characterized by $C(V) = \frac{C_{jo}}{\left[1+\frac{V}{\phi_b}\right]^{m_j}}$, while, for linear capacitors, $C_d = \langle C_{eff}\rangle = C_{jo}$.
[3]Note that, in (13), $\alpha(y) \equiv y\cot(y) - 1$.

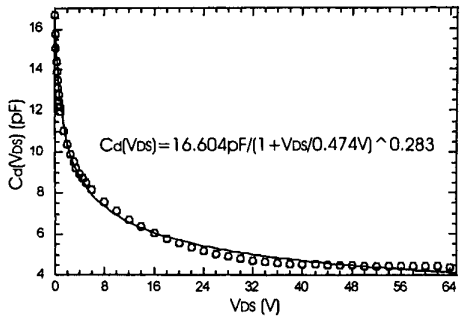

Fig. 3. CV Profile for Ericsson PTF-10135 LDMOS FET

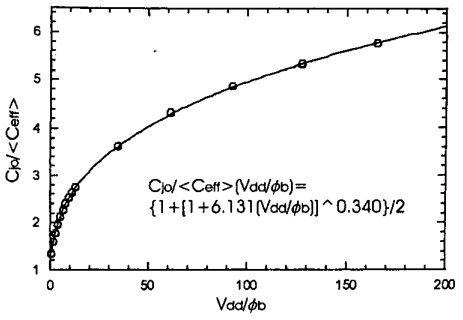

Fig. 4. Plot and Best Fit of $\frac{C_{jo}}{\langle C_{eff}\rangle}$ versus $\frac{V_{dd}}{\phi_b}$

$$R_L = \frac{2V_{dd}^2}{P_{out}} \frac{\sin^2(y)}{\left[y^2 + \left(\alpha(y) + \frac{\sigma\omega C_{jo}}{I_{dc}}\right)^2\right]} \tag{15}$$

$$\begin{aligned} L_X = \frac{X}{\omega} = & \frac{R_L}{\omega\left[\alpha(y) + \frac{\sigma\omega C_{jo}}{I_{dc}}\right]} \\ & \left[y - \frac{\alpha^2(y) + y^2 + \left(\frac{\sigma\omega C_{jo}}{I_{dc}}\right)^2}{2y} \right. \\ & \left. \left(1 + \frac{1 - [y\csc(y)]^2}{\alpha(y)}\right)\right] \end{aligned} \tag{16}$$

Now all that is left is to derive the relationship between R, R_L, and L_f.

C. Design Equations for L_f

At the resonant frequency of the LC series-tuned circuit (labeled as "BPF" in figs. 1&2),

$$Z'_{out} = \frac{Q_f^2 R + j\omega L_f}{1 + Q_f^2}, \tag{17}$$

since L_f shunts R. Separately equating the real and imaginary parts of (17) to the series equivalent form,

$$Z'_{out,series} = R_L + j\omega L'_f, \tag{18}$$

results in[4]

$$R_L = \frac{Q_f^2}{1 + Q_f^2} R \tag{19}$$

and

$$L'_f = \frac{L_f}{1 + Q_f^2}, \tag{20}$$

[4]Again, please note that R_L is the Class E load resistance, which is not to be confused with $R = 50\Omega$.

subject to the constraint,

$$\omega L'_f \leq X, \tag{21}$$

since

$$X = \omega(L'_X + L'_f). \tag{22}$$

III. Experimental Results

The validity of this implementation of the finite DC feed inductor was verified experimentally using a silicon LDMOS FET device[5] at $200MHz$[6] with $\sigma = 0$ and $y = 0.55\pi$ (45 percent duty-cycle). Since this FET device exhibits a highly nonlinear output capacitance (see fig. 3) this report also offers experimental verification of the design methodology for Class E power amplifiers with nonlinear output capacitors proposed in [9] and [10], and shows that this finite feed approach is independent of the capacitor's nonlinearity.

Since the junction grading coefficient, $m_j = \frac{n}{n+1} = 0.283$, cannot be represented by a positive integer value[7] of n, the numerical approach described in [9] and [10] was used to generate the plot (see fig. 4) and best fit equation relating C_{jo} to $\langle C_{eff}\rangle$ and ϕ_b,

$$\frac{C_{jo}}{\langle C_{eff}\rangle} = \frac{1}{2}\left[1 + \left(1 + 6.131\frac{V_{dd}}{0.474V}\right)^{0.340}\right], \tag{23}$$

through numerically calculated values of V_{dd}.

Using $V_{dd} = 12V$ in (23) results in $\langle C_{eff}\rangle = 5.05pF$, which can be used in (14)–(16), to compute the component values. These values can then be used to compute the appropriate values for L_f and L'_X, by using (19), (20), and (22), see table I.

[5]The Ericsson PTF-10135 is rated for $5W$, $V_{BR,DSS} = 65V$.

[6]$200MHz$ was chosen to strike a balance between the transistor's transconductance and $\langle C_{eff}\rangle$, see (14), and to facilitate the realization of the inductors.

[7]In [9] and [10], it was shown that closed form, analytic solutions are possible for $n = 1, 2, 3, \ldots$.

V_{dd}	P_{out}	R_L	L_X
$12V$	$1.77W$	34.4Ω	$37.9nH$
L	C	L_f	L'_X
$137nH$	$4.62pF$	$59.2nH$	$19.9nH$

TABLE I

DESIGN PARAMETERS AND COMPONENT VALUES FOR $f = 200MHz$, $y = 0.55\pi$, $\sigma = 0$, AND $Q_L = 5$

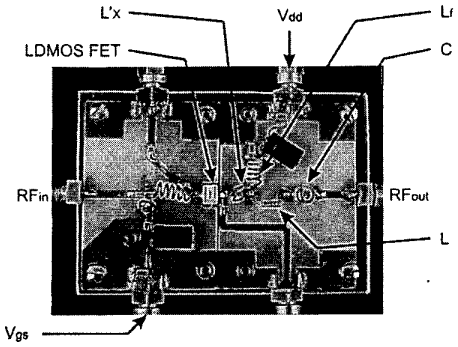

Fig. 5. $200MHz$ Class E Power Amplifier Prototype

The maximum efficiency was $\eta_{max} = 77.35\%$, but with gain of only $7.52dB$, resulting in $PAE = 63.66\%$ ($P_{out} = 1.41W$ and $P_{dc} = 1.83W$), see fig. 6. At a lower input level, the peak PAE was 74.29%, with an associated efficiency of 75.22%. In this case, $P_{out} = 1.31W$, with $P_{dc} = 1.74W$ which matches the design value of $1.77W$ quite well. Approximately 12.5% power loss can be attributed to the finite ON resistance of the device, $V_{DS,ON} \approx 1.5V$, while the output resonator's parasitic resistance is believed to be responsible for the remainder of the power loss[8].

IV. CONCLUSION

A set of simple design equations were derived and applied to a Class E power amplifier with a finite DC feed inductor that provided complex load transformation, in addition to supplying the DC connection. The proposed method is independent of the output capacitor's voltage dependence, and was verified experimentally using a silicon LDMOS FET that produced a maximum $PAE = 74.29\%$ with an associated $\eta = 75.22\%$ ($P_{out} = 1.31W, P_{dc} = 1.74W$) at $200MHz$.

[8] L in fig. 5 is an air-core inductor (16 turns, 34 gauge wire, $1.8mm$ diameter). Previous attempts using a toroidal inductor wound on a ferrite core, resulted in roughly $3dB$ reduction in P_{out}, and using a chip inductor resulted in about $1.25dB$ reduction. The loss in the air-core inductor could plausibly account for the remaining $0.5dB$ difference between P_{dc} and P_{out}.

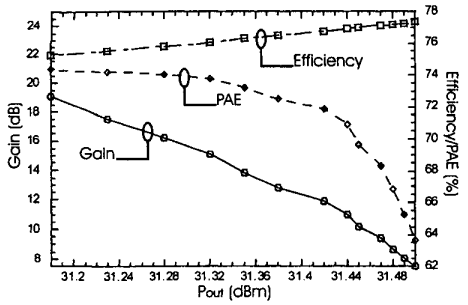

Fig. 6. Plot of Gain, η, and PAE versus P_{out}

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