Transactions Briefs

The Effect of Transistor Feedback Capacitance in Class-E Power Amplifiers

David K. Choi and Stephen I. Long

***Abstract*—In this brief, the contribution of transistor feedback capacitance to the total output capacitance in Class-E power amplifiers is analyzed. It is shown that the feedback capacitance loads the output of the transistor by its nominal value plus an amount proportional to the ratio of the input voltage amplitude to the peak voltage across the output of the transistor. Because a high-input drive is required for good transistor switching action, high-voltage swings may be present at the input, and so this effect should not be neglected. Computer simulations are used to verify the validity of this analysis by comparing the cases without feedback capacitance, with feedback capacitance, and where the effect of the feedback capacitance is accounted for using the design equation derived in this report.**

***Index Terms*—FET amplifiers, MOSFET power amplifiers, switching amplifier, ultrahigh frequency (UHF) power amplifiers.**

I. Introduction

The effects of various transistor device parasitics on the operation of the Class-E power amplifier [1] have been analyzed in the literature. Several reports have examined the effect of the voltage dependence of the output capacitance [2]–[5], while others have examined the effect of finite ON resistance [6] and input resistance [7]. This report is dedicated to an approximate analysis of the transistor feedback capacitance [$C_{\rm gd}$ in FETs, C_{bc} in bipolar junction transistors (BJTs)], with the goal of providing a revised design equation for the Class-E output capacitance that accounts for the effect of the transistor feedback capacitance.

II. Analysis

An idealized Class-E power-amplifier circuit is shown in Fig. 1. For simplicity, the series LC resonator ("BPF" in Fig. 1) is assumed to have an infinite Q (so that i_o is a single-tone sinusoid) and the transistor is assumed to operate as an ideal switch, cycling between an open and short circuit with duty cycle $D \in (0,1)$ defined as

$$D = 1 - \frac{y}{\pi} \tag{1}$$

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where $2y \in (0, 2\pi)$ is defined as the nonconduction angle, [1] see Fig. 2. The conduction interval ($\theta_{\rm on} \le \theta < \theta_{\rm off}$) and the nonconduction interval ($\theta_{\rm off} \le \theta < \theta_{\rm on}$), where $\theta = \omega t$, are delineated by

$$\begin{aligned}\theta_{\rm on} &= y - \frac{\pi}{2}, \frac{3\pi}{2} + y, \ldots \\ \theta_{\rm off} &= \frac{3\pi}{2} - y, \frac{7\pi}{2} - y, \ldots .\end{aligned} \tag{2}$$

In Fig. 1, the feedback capacitor, $C_{\rm gd}$, appears between the input (control port, $v_{\rm GS}$) and output port ($v_{\rm DS}$) of the switch. The contribution of $C_{\rm gd}$ to the total output capacitance during the nonconduction interval will be analyzed below.

A. Approximating $v_{\rm DS}$ With a Sinusoidal Pulse

The exact mathematical form of $v_{\rm DS}$ (shown in Fig. 2) as a function of $V_{\rm DD}$, y, and θ [8] is shown in (3) at the bottom of the page, where it was assumed that the output capacitance is voltage independent and the slope of $v_{\rm DS}$ at the onset of conduction (defined as σ) is zero, and where

$$\alpha(y) \equiv y\cot(y) - 1. \tag{4}$$

But for the sake of simplicity, $v_{\rm DS}$ will be approximated by a sinusoidal pulse

$$\begin{aligned} v_{\rm DS}(\theta) &\approx \\ v_{\rm sine}(\theta) &= \begin{cases} 0, & \theta_{\rm on} \le \theta < \theta_{\rm off} \\ \frac{v_{\rm DS,max}[\sin(\theta-\pi)+\cos(\pi D)]}{1+\cos(\pi D)}, & \theta_{\rm off} \le \theta < \theta_{\rm on} \end{cases} \end{aligned} \tag{5}$$

where, the peak value of $v_{\rm DS}$

$$v_{\rm DS,max} \equiv v_{\rm DS}(\theta)|_{\theta_{\rm max}} \tag{6}$$

can be computed from (3) using $\theta_{\rm max}$ [5] and [8]

$$\theta_{\rm max}|_{\sigma=0} = \pi + \arcsin\left(\frac{\sin(y)}{\sqrt{y^2+\alpha^2(y)}}\right) - \arctan\left(\frac{\alpha(y)}{y}\right). \tag{7}$$

Fig. (3a)–(c) compares the normalized voltage waveforms of the exact value of $v_{\rm DS}$ in (3) versus the sinusoidal approximation given in (5). Although there is a shift between the peaks of the waveforms, their shapes are adequate to serve as approximations.

B. Feedback Effect of $C_{\rm gd}$ (Nonconduction Interval)

The input stimulus $v_{\rm GS}$ can be expressed as

$$\begin{aligned} v_{\rm GS}(\theta) &= V_{\rm BIAS} + V_{\rm in,max}\sin(\theta) \\ &= V_{\rm th} + V_{\rm in,max}\left[\sin(\theta) - \cos(\pi D)\right]. \end{aligned} \tag{8}$$

[1] $2x$ is the conduction angle, and $x + y = \pi$.

$$v_{\rm DS}(\theta)|_{\sigma=0} = \begin{cases} 0, & \theta_{\rm on} \le \theta < \theta_{\rm off} \\ \frac{\pi V_{\rm DD}}{\alpha^2(y)}\left\{\theta - \frac{3\pi}{2} + \csc(y)\left[\alpha(y)\left[\sin(\theta)+\cos(y)\right] - y\cos(\theta)\right]\right\}, & \theta_{\rm off} \le \theta < \theta_{\rm on} \end{cases} \tag{3}$$

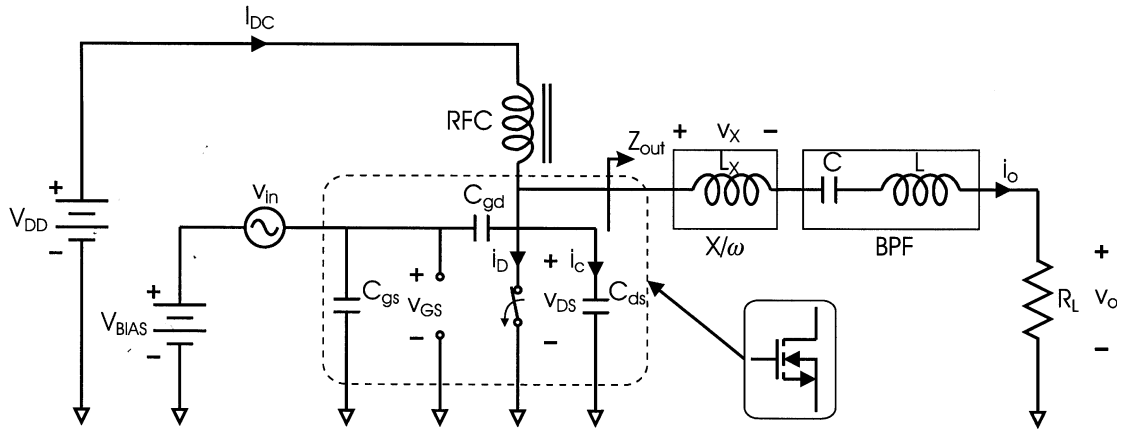

Fig. 1. Idealized Class-E power-amplifier circuit with transistor's parasitic capacitors.

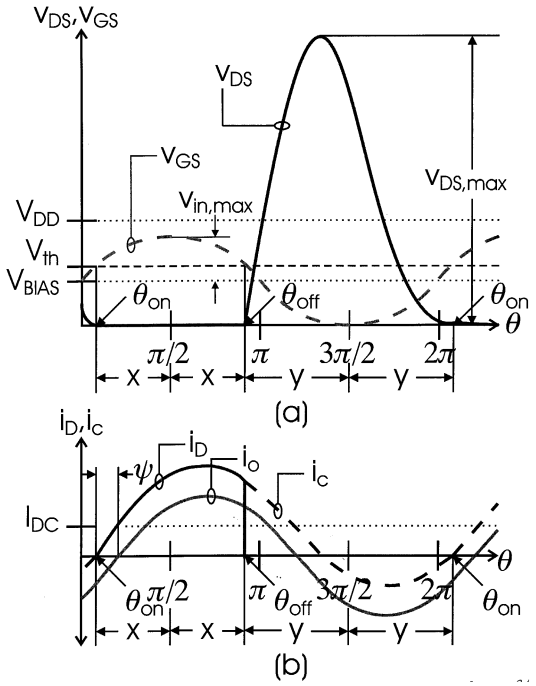

Fig. 2. Class-E waveforms. (a) Switch input drive ($v_{\rm GS}$) and switch output port voltage ($v_{\rm DS}$). (b) Switch current (i_D), capacitor current (i_c), and output current (i_o).

Applying (5) and (8) to the equivalent circuit in Fig. 1, the output referred loading effect of the feedback capacitor $C_{\rm gd}$ is given by

$$C_{\rm gd,eq} = C_{\rm gd}\left[1 + \frac{V_{\rm in,max}\,(1+\cos(\pi D))}{v_{\rm DS,max}}\right]. \tag{9}$$

The total output capacitance can now be written as

$$C_{\rm out} = C_{\rm ds} + C_{\rm gd}\left[1 + \frac{V_{\rm in,max}\,(1+\cos(\pi D))}{v_{\rm DS,max}}\right] \tag{10}$$

which should be used to insure that the combined values of $C_{\rm ds}$ and $C_{\rm gd}$ correspond to the Class-E output capacitance, as expressed in (12).

III. Simulation Results

To verify the validity of this analysis, simulations of the Class-E power-amplifier circuit (see Fig. 1), using ideal lumped elements and an ideal switch[2] in place of the transistor, were performed under the following three conditions:

1) without feedback capacitance;
2) with feedback capacitance, $C_{\rm gd}$;
3) with feedback capacitance, $C'_{\rm gd}$, as corrected by (10).

The design parameters[3] for the simulations were: $f = 1$ GHz, $V_{\rm DD} = 9\ V$, $P_{\rm out} = 2\ W$, $Q_L = 7$. For the sake of brevity, only the results using a 50% duty cycle are shown. In addition to qualitative indicators,[4] efficiency $(\eta = (P_{\rm out})/(P_{dc}))$ and the voltage at the onset of conduction

$$v_{\rm DS,on} \equiv v_{\rm DS}(\theta)|_{\theta=\theta_{\rm on}} \tag{11}$$

quantify how well the circuits operate under each of the three conditions.

Derivations of the optimum Class-E output capacitance and the remaining Class-E circuit elements in Fig. 1 (L_X, L, C, and R_L) are beyond the scope of this work, but are worked out in detail in [5] and [8]. They are included here[5] for the sake of completeness.

$$C_{\rm out} = \frac{P_{\rm out}\alpha^2(y)}{\pi\omega V_{\rm DD}^2} \tag{12}$$

$$R_L = \frac{2\left[V_{\rm DD}\sin(y)\right]^2}{P_{\rm out}\left[y^2+\alpha^2(y)\right]} \tag{13}$$

$$L_X = \frac{1}{\omega\alpha(y)}\left\{y + \frac{y\csc^2(y) - \cot(y)}{2\alpha(y)}\left[y^2+\alpha^2(y)\right]\right\}R_L \tag{14}$$

$$L = \frac{Q_L R_L}{\omega} \tag{15}$$

$$C = \frac{1}{\omega^2 L}. \tag{16}$$

[2]The switch ON resistance was set to 1 mΩ and the OFF resistance was set to 1 MΩ.

[3]$Q_L \equiv (\omega L)/(R_L)$.

[4]Under proper Class-E operation, the voltage waveform should go to zero with the correct slope [1].

[5]These expressions (12)–(16), (3), (6), and (7), assume that $v_{\rm DS}$ goes to zero with zero slope (soft switching), the design equations that allow for nonzero voltage slope are derived in [5], [8].

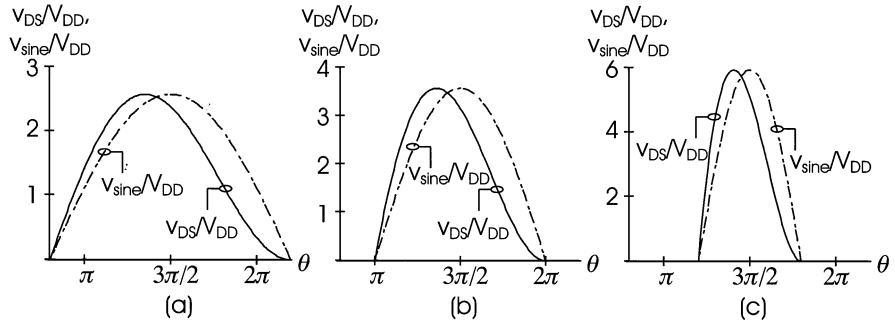

Fig. 3. Normalized waveforms for comparisons of actual drain voltage $v_{\rm DS}$ versus approximation as a sinusoidal pulse $v_{\rm sine}$ for: (a) 30 percent duty cycle; (b) 50 percent duty cycle; (c) 70 percent duty cycle.

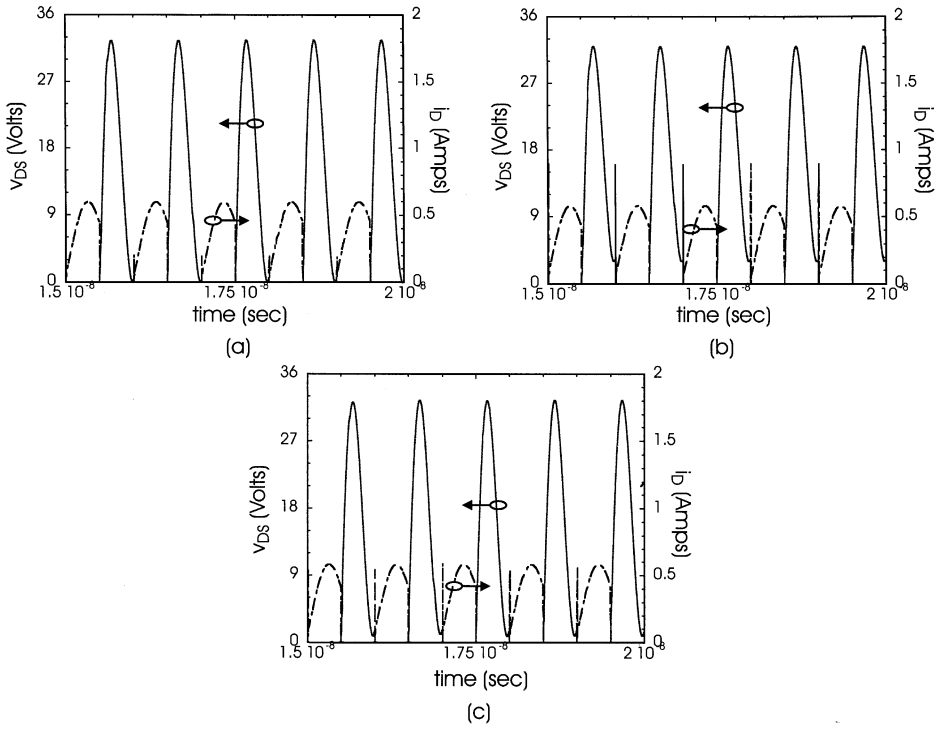

Fig. 4. Simulated $v_{\rm DS}$ and i_D waveforms versus θ. (a) Without $C_{\rm gd}$. (b) With $C_{\rm gd}$. (c) With $C'_{\rm gd}$($f = 1$ GHz, $P_{\rm out} = 2\ W$, $V_{\rm DD} = 9\ V$, $Q_L = 7$, $D = 0.5$, $\sigma = 0$).

TABLE I
COMPONENT VALUES AND SIMULATION RESULTS ($f = 1$ GHz, $V_{\rm DD} = 9$ V, $P_{\rm out} = 2\ W$, $Q_L = 7$, $D = 0.5$, $\sigma = 0$)

	w/o C_{gd}	w/ C_{gd}	w/ C'_{gd}
C_{ds}	$1.251pF$	$1.000pF$	$1.000pF$
C_{gd}	—	$0.251pF$	$0.154pF$
P_{out}	$1.987W$	$1.895W$	$1.919W$
P_{DC}	$1.993W$	$1.982W$	$1.989W$
η	99.7%	95.6%	96.5%
$v_{DS,max}$	$32.60V$	$31.54V$	$31.97V$
$v_{DS,on}$	$0.344V$	$2.965V$	$1.651V$

The resultant current and voltage waveforms from the simulations i_D and $v_{\rm DS}$, respectively, are shown in Fig. 4. The values of $C_{\rm ds}$ and $C_{\rm gd}$ and the values for $P_{\rm out}$, P_{DC}, $\eta = (P_{\rm out})/(P_{DC})$, $v_{\rm DS,max}$, and $v_{\rm DS,on}$ are shown in Table I. The waveforms in Fig. 4(a), depicting the case with no feedback capacitance, show that the circuit is properly designed, while the values, $\eta = 99.7\%$ and $v_{\rm DS,on} = 0.344$ V, in Table I confirm that the simulation approaches ideal operation.

The circuit used to generate the waveforms in Fig. 4(b) differs from the one used in Fig. 4(a) in that a 0.251-pF feedback capacitor[6] was added, while $C_{\rm ds}$ was reduced by the same amount. The voltage waveform in Fig. 4(b) is close to 3 V when the switch turns on, indicating that the circuit is not properly designed, and results in a large discharging current spike. The simulation from which the waveforms in Fig. 4(c) are obtained differs from that used for Fig. 4(b) in that the value of $C_{\rm gd}$ was corrected according to the expression in (10). The new value $C'_{\rm gd} = 0.154$ pF was computed[7] by using $C_{\rm gd} = 0.251$ pF, $v_{\rm DS,max} = 32.60$ V, and $V_{\rm in,max} = 20$ V (same input drive used for all simulations[8]) in (10).

[6]Under the Class-E operating conditions considered here, the ratio between $C_{\rm gd}$ and $C_{\rm ds}$ can vary from about 1:6 to 1:30 (both are strongly nonlinear) for practical MOSFET devices [9], while ratios around 1:4 are reasonable for MESFETs [10]. Here, the value of $C_{\rm gd} = 0.251$ pF was chosen for convenience, so that $C_{\rm ds} = 1$ pF.

[7]$C'_{\rm gd}$ is the value that, when substituted for $C_{\rm gd}$ in (10), gives the correct value of $C_{\rm out}$, according to (12).

[8]20 V gate-voltage swings, while quite high, can be tolerated by LDMOSFET devices [9].

The waveforms in Fig. 4(c) reveal that the correction in (10) is only approximate, but yields a definite improvement over that in Fig. 4(b). Using $C'_{\rm gd} = 0.154$ pF reduces $v_{\rm DS,on}$ to 1.651 V, from 2.965 V, with a corresponding improvement in efficiency from 95.6% to 96.5%. Tuning the circuit of Fig. 4(c) by trial and error shows that if L_X in Fig. 1 is changed from 4.285 nH, as computed from (14), to 4.775 nH, nearly ideal waveforms like those shown in Fig. 4(a) can be obtained. Without changing the values of $C'_{\rm gd} = 0.154$ pF or $C_{\rm ds} = 1.000$ pF, this simulation yielded the following values: $P_{\rm out} = 1.960$ W, $P_{DC} = 1.965$ W, $\eta = 99.7\%$, $v_{\rm DS,max} = 35.47$ V. The reduction in $P_{\rm out}$ and P_{dc} indicate that $C_{\rm out}$, as computed from (12), is slightly underestimated. Furthermore, the fact that adjusting only L_X produced the correct operation is indicative of another error in the approximation in (9); in this case, in the phase of $v_{\rm DS}$, which is controlled by L_X.

IV. Conclusion

The goal of this brief was to develop conceptual understanding of the feedback effect of $C_{\rm gd}$ and to derive a simple, approximate design equation taking the feedback effect into account for initial design. It is a given that, in practice, the power-amplifier design will have to be optimized in successive design iterations. The intent is, therefore, that the design equation derived in this report, (10), will serve as a starting point, while the intuitive insights developed in the theoretical analysis will provide the basis for final design optimization.

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A New Method for Harmonic Distortion Analysis in Class-AB Stages

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***Abstract*—In this brief, a new method for analytically evaluating the harmonic distortion (HD) in class-AB stages is introduced. It is based on modeling each push–pull device in the stage with a different third-order polynomial. The coefficients of these polynomials are then evaluated by straightforward computations or by pencil-and-paper analysis on the transcharacteristic of the stage. The resulting theory was validated by simulations and is able to predict the HD behavior of a class-AB stage over a wide range of input values. An example of the use of the theory for pencil-and-paper analysis is also given.**

***Index Terms*—Amplifier distortion, analog circuits, harmonic analysis, harmonic distortion (HD), nonlinear circuits, operational amplifiers.**

I. Introduction

Total harmonic distortion (THD) can be viewed as value measuring the amount of energy in the harmonics, relative to the energy in the fundamental [1], Y_k being the *magnitude* of the kth harmonic and naming the kth harmonic distortion (HD) component as $\mathrm{HD}_k = Y_k/Y_1$, THD is often well approximated by $\mathrm{THD} \simeq \sqrt{\mathrm{HD}_2^2 + \mathrm{HD}_3^2}$.

An important class of circuits where distortion must be taken into account during the design phase are class-AB stages. In fact, these blocks work under the large-signal condition and the nonlinearity of their active elements is main factor responsible for the HD in operational amplifiers [2]–[5] or in current-mode circuits [6], [7]. Unfortunately, despite its importance, designers seldom evaluate distortion analytically and its determination is often left to simulations or to vague considerations about circuit symmetry. This inevitably leads to a nonoptimized circuit design where distortion is frequently minimized by increasing the gain of the feedback loop where the stage is placed. Analytical evaluation of distortion is a fundamental task used, for example, for comparing new topologies, for evaluating the distortion sensitivity to a parameter change, or for improving performance of a given class-AB stage. Consequently, having a mathematical model for HD allows designers to better understand the behavior of class-AB stages and gives them a powerful tool of analysis for improving circuit performances.

The literature reports some methods for evaluating THD analytically in terms of HD_2 and HD_3, but they present some weaknesses. The first method can be found in [8] and is used, for example, in [9] and [10]. It predicts HD_2 and HD_3 values, only for a sinusoidal input amplitude equal to X_M. Hence, if we need to quantify the distortion for a different amplitude, the method must be applied again with a different value for X_M. Moreover, it assumes low distortion and does not give accurate results if the original transcharacteristic significantly deviates from a third-order polynomial, which is common in class-AB stages where push–pull topologies are adopted.

The second method was first introduced in [11]–[13] and used in [14] to evaluate the distortion of CMOS current mirrors. The method is slightly more accurate than the previous one, but, in this case too, it predicts distortion only for a sinusoidal input amplitude equal to X_M.

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